604-Pin Socket

Design Guidelines

October 2002

Order Number: 273769-001

Contents

Figures

Tables

Revision History

Date	Revision	Description
October 2002	001	Initial release of this document.

This page intentionally left blank.

1.0 Introduction

1.1 Objective

This document defines a surface mount, Zero Insertion Force (ZIF) socket intended for workstation and server platforms based on future Intel microprocessors. The socket provides I/O, power and ground contacts. The socket contains 604 contacts arrayed about a cavity in the center of the socket with solder balls/surface mount features for surface mounting with the motherboard. The 604-pin Socket contacts have 50 mil pitch with regular pin array, to mate with a 604-pin processor package. FC-mPGA2 and INT_mPGA packages may be mated with the 604-pin Socket. The mechanical keying pin is a key that allows either the 603-pin processor package or the 604-pin processor package to be used in the same socket.

1.2 Purpose

To define functional, quality, reliability, and material (e.g., visual, dimensional and physical) requirements and design guidelines of the 604-pin Socket in order to provide low cost, low risk, robust, high volume manufacturing (HVM) socket solution available from multiple sources.

1.3 Scope

This document specifies design guidelines for 604-pin ZIF sockets.

This page intentionally left blank.

2.0 Assembled Component and Package Description

Information provided in this section is to ensure dimensional compatibility of the 604-pin Socket with that of the 604-pin processor package. The processor package must be inserted into the 604-pin Socket with zero insertion force when the socket is not actuated.

2.1 Assembled Component Description

The assembled component may consist of a heatsink, EMI shield, clips, fan, retention mechanism (RM), and processor package. Specific details may be obtained from Thermal Design Guidelines. Visit the Intel World Wide Web site at http://www.intel.com, or contact your Intel field representative.

2.2 Package Description

The pin-out for the 604-pin processor package is shown in Figure 9, “42.5 mm, 604-Pin Package Assembly Drawing” on page 40 (Appendix A).

The pin dimension details, base material, plating material and plating thickness are shown in Figure 10, “42.5 mm, 604-Pin Package Assembly Drawing with Package Detail” on page 41 (Appendix A). Note the dimensional variation when designing to ensure ZIF. The package Critical To Function (CTF) Dimensions are presented in Table 1. CTF values are detailed on the processor package drawings and take precedence over all values presented in this document.

Table 1. Package Critical To Function (CTF) Dimensions

Dimension
Shoulder Diameter (Land Solder Fillet Shoulder Inclusion)
Pin Diameter
Shoulder Diameter Protrusion (Land Solder Fillet Shoulder Inclusion)
Pin Length (Effective)†
Pin True Position (Pattern Relating and Feature Relating)†
Flatness of Processor†

† Pin length, Pin True Position and Flatness tolerances are controlled by Geometric Dimensioning and Tolerance (GD and T) controls.

This page intentionally left blank.

3.0 Mechanical Requirements

3.1 Mechanical Supports

A retention system needs to isolate any load in excess of 50 lbf, compressive, from the socket during the shock and vibration conditions outlined in Section 5.0, “Environmental Requirements” on page 27. The socket must pass the mechanical shock and vibration requirements listed in Section 5.0 with the associated heatsink and retention mechanism attached. The socket may only be attached by the 603 contacts to the motherboard. No external methods (i.e., screw, extra solder, adhesive, etc.) to attach the socket are acceptable.

3.2 Materials

3.2.1 Socket Housing

Thermoplastic or equivalent, UL* 94V-0 flame rating, temperature rating, and design capable of withstanding a temperature of 240° C for 40 seconds (minimum) typical of a reflow profile for solder material used on the socket. The material must have a thermal coefficient of expansion in the XY plane capable of passing reliability tests rated for an expected high operating temperature, mounted on FR4-type motherboard material.

3.2.2 Color

The color of the socket may be optimized to provide the contrast needed for OEMs pick and place vision systems. The base and cover of the socket may be different colors as long as they meet the above requirement.

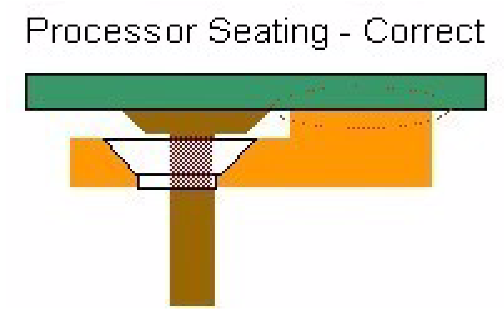
3.3 Cutouts for Package Removal

Recessed cutouts are required in the side of the socket to provide better access to the package substrate, and facilitate the manual removal of inserted package. See Figure 13, “mPGA604 Socket Drawing with Dimensions (Continued)” on page 44 (Appendix A) for more information.

3.4 Socket Standoff Height

Socket stand off height, cover lead in and cover lead in depth must not interfere with package pin shoulder at worst case conditions. The processor (not the pin shoulder) must sit flush on the socket standoffs and the pin field cannot contact the standoffs, as shown in Figure 1. See Figure 12, “mPGA604 Socket Drawing with Dimensions” on page 43 (Appendix A) for more information.

Figure 1. Processor Seating-Correct



3.5 Markings

All markings required in this section must be able to withstand a temperature of 240° C for 40 seconds (minimum) typical of a reflow profile for solder material used on the socket, as well as any environmental test procedure outlined in Section 5.0.

3.5.1 Name

mPGA604 (Font type is Helvetica Bold – minimum 6 point).

This mark shall be molded or Laser Marked into the processor side of the socket housing.

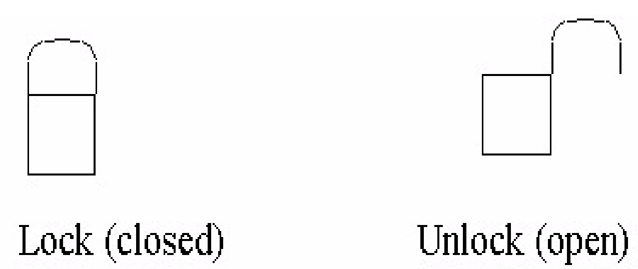
Manufacturer's insignia (font size at supplier's discretion).

This mark may be molded or laser marked into the socket housing. Both marks must be visible when first seated in the motherboard. Any request for variation from this marking requires a written description (detailing size and location) to be provided to Intel for approval.-P

3.5.2 Lock (closed) and Unlock (open) Markings

The universal symbols for 'Lock' and 'Unlock' are to be marked on the socket in the appropriate positions, as shown in Figure 2. Clear indicator marks must be located on the actuation mechanism that identifies the lock (closed) and unlock (open) positions of the cover as well as the actuation direction. These marks should still be visible after a package is inserted into the socket.

Figure 2. Universal Symbols for Lock and Unlock



3.5.3 Lot Traceability

Each socket may be marked with a lot identification code that may allow traceability of all components, date of manufacture (year and week), and assembly location. The mark must be placed on a surface that is visible when mounted on a printed circuit board. In addition, this identification code must be marked on the exterior of the box in which the units ship.

3.6 Socket Size

The socket size must meet the dimensions as shown in Figure 12, “mPGA604 Socket Drawing with Dimensions” on page 43 (Appendix A), and Figure 13, “mPGA604 Socket Drawing with Dimensions (Continued)” on page 44 (Appendix A), allowing full insertion of the pins in the socket, without interference between the socket and the pin field. The 604-pin Socket and actuation area must fit within the keep-in zone defined in Figure 13, “mPGA604 Socket Drawing with Dimensions (Continued)” on page 44 (Appendix A).

3.7 Socket / Package Translation During Actuation

The socket shall be built so that the post-actuated package pin field displacement may not exceed 1.27mm. Movement may be along the Y direction (refer to axes as indicated in Figure 12, “mPGA604 Socket Drawing with Dimensions” on page 43 (Appendix A). No Z-axis travel (lift out) of the package is allowed during actuation.

3.8 Orientation in Packaging and Shipping and Handling

Packaging media needs to support high volume manufacturing.

3.9 Contact Characteristics

3.9.1 Number of Contacts

Total number of contacts: 603

Total number of contact holes: 604

3.9.2 Base Material

High strength copper alloy

3.9.3 Contact Area Plating

A layer of gold plating that is 0.762 µm (minimum) thick over nickel underplate that is 1.27 µm (minimum) thick in critical contact areas (the area on socket contacts where processor pins may mate) is required. No contamination by solder in the contact area is allowed during solder reflow.

3.9.4 Solder Ball Attachment Area Plating

3.81 µm (minimum) Tin/Lead (typically 85 ±5 Sn/15Pb)

3.9.5 Solder Ball Characteristics

Tin/Lead (63/37 ± 0.5% Sn)

3.9.6 Lubricants

For the final assembled product, no lubricant is permitted on the socket contacts. When lubricants are used elsewhere within the socket assembly, these lubricants must not be able to migrate to the socket contacts.

3.10 Material and Recycling Requirements

Cadmium shall not be used in the painting or plating of the socket.

CFCs and HFCs shall not be used in manufacturing the socket. It is recommended that any plastic component exceeding 25 grams must be recyclable as per the European Blue Angel recycling design guidelines.

3.11 Lever Actuation Requirements

- Lever closed direction – right
- Actuation direction called out in Figure 12, “mPGA604 Socket Drawing with Dimensions” on page 43 (Appendix A)
- 135° lever travel maximum
- Pivot point in the center of the actuation area on the top of the socket. See Figure 13, “mPGA604 Socket Drawing with Dimensions (Continued)” on page 44 (Appendix A) for more information.

3.12 Socket Engagement/Disengagement Force

The force on the actuation lever arm must not exceed 44 N to engage or disengage the package into the 604-pin Socket. Movement of the cover is limited to the plane parallel to the motherboard. The processor package must not be utilized in the actuation of the socket. Any actuation must meet or exceed SEMI* S8-95 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment, example Table R2-7 (Maximum Grip Forces).

3.13 Visual Aids

The socket top may have markings identifying Pin 1. This marking may be represented by a clearly visible triangular symbol. See Figure 13, “mPGA604 Socket Drawing with Dimensions (Continued)” on page 44 (Appendix A) for more information.

3.14 Socket BGA Co-Planarity

The co-planarity (profile) requirement for all solder balls on the underside of the socket is located in Figure 12, "mPGA604 Socket Drawing with Dimensions" on page 43 (Appendix A) for more information.

3.15 Solder Ball True Position

The solder ball pattern has a true position requirement with respect to Datum A, B, and C. See Figure 12, "mPGA604 Socket Drawing with Dimensions" on page 43 (Appendix A) for more information.

3.16 Critical to Function Dimensions

The 604-pin Socket shall accept a 604-pin processor pin field. All dimensions are in metric units. Asymmetric features are designed to properly align the socket to the motherboard and prevent the socket from being assembled incorrectly to the motherboard.

CTF (Critical to Function) dimensions are identified in Table 2. The CTF values are detailed on the 604-pin Socket drawing in Figure 12, "mPGA604 Socket Drawing with Dimensions" on page 43 (Appendix A) and Figure 13, "mPGA604 Socket Drawing with Dimensions (Continued)" on page 44 (Appendix A) and take precedence over all values presented in this document. Dimensional requirements identified in the drawings and in Table 2 must be met. These dimensions will be verified as part of the validation process. Also, the supplier will provide and maintain Critical Process Parameters (CPP) controlling these CTFs, or will provide direct measurements to meet ongoing quality requirements.

Table 2. Socket Critical to Function Dimensions

Dimension
Socket Length
Socket Width
Socket Height (Interposer surface from MB)
Assembled Seating Plane Flatness
Ball Diameter
True Position of Balls (pattern relating)
Co-planarity (profile) of Balls
Actuation Distance (Cover Travel)
Through Cavity X
Through Cavity Y
Cover Hole Diameter (Must ensure ZIF)
Cover Hole Countersink Depth (Must ensure ZIF)
Cover Hole Countersink Diameter (Must ensure ZIF)
Cover Hole Virtual Condition (Pattern Locating)
Cover Hole Virtual Condition (Feature Relating)
Cover Hole Field Depth wrt Seating Plane
Cover Thickness in Hole area
Au Thickness
Ni Thickness
Alignment Post Virtual Condition
Contact Depth from Seating Plane

4.0 Electrical Requirements

Socket electrical requirements are measured from the socket-seating plane of the processor test vehicle (PTV) to the component side of the socket PCB to which it is attached. All specifications are maximum values (unless otherwise stated) for a single socket pin, but includes effects of adjacent pins where indicated. Pin and socket inductance includes exposed pin from mated contact to bottom of the processor pin field.

Table 3. Electrical Requirements for Sockets

Section	Requirement	Value	Reference
1	Mat11 loop inductance, Lloop	<4.33 nH	Refer to Table 4 section 1.
2	Mated partial mutual inductance, L	NA	Refer to Table 4 section 2.
3	Maximum mutual capacitance, C	<1 pF	Refer to Table 4 section 3.
4	Maximum Ave Contact Resistance	$\leq$ 17 mΩ	Refer to Table 4 section 4. Refer to Section 4.1 for more detail. Refer to the *µPGA603 Socket Design Guidelines* for electrical parameters with INT3 packages.
5	Measurement frequencies for Pin-to-Pin/ Connector-to-Connector capacitance.	400 MHz	
6	Measurement frequencies for Pin-to-Pin/ Connector-to-Connector inductance.	1 GHz	
7	Dielectric Withstand Voltage	360 V_{RMS}	
8	Insulation Resistance	800 MΩ	
9	Contact Current Rating	Read and record	

Table 4. Definitions

Section	Requirement	Definition
1	Mated loop inductance, Lloop. Refer to Table 3, section 1.	The inductance calculated for two conductors, considering one forward conductor and one return conductor.
2	Mated mutual inductance, L. Refer to Table 3, section 2.	The inductance on a conductor due to any single neighboring conductor.
3	Maximum mutual capacitance, C. Refer to Table 3, section 3.	The capacitance between two pins/connectors.
4	Maximum Average Contact Resistance Refer to Table 3, section 4.	The maximum average resistance target is originally derived from maximum resistance of each chain minus resistance of shorting bars divided by number of pins in the daisy chain. This value has to be satisfied at all time. Thus, this is the specification valid at End of Line, End of Life, etc. **Socket Contact Resistance:** The resistance of the socket contact, interface resistance to the pin, and the entire pin to the point where the pin enters the interposer; gaps included.
5	Measurement frequencies for capacitance.	Capacitively dominate region. This is usually the lowest measurable frequency. This should be determined from the measurements done for the feasibility.
6	Measurement frequencies for inductance.	Linear region. This is usually found at higher frequency ranges. This should be determined from the measurements done for the feasibility.

4.1 Electrical Resistance

Figure 3 and Figure 4 show the proposed methodology for measuring the final electrical resistance. The methodology requires the measuring interposer be flush-mounted directly to the motherboard fixtures, so that the pin shoulder is flush with the motherboard to obtain the averaged jumper resistance, R_{jumper}. The R_{jumper} should come from a good statistical average of 30 package fixtures flush mounted to a motherboard fixture. The same measurements are then made with a package fixture mounted on a supplier's socket, and both are mounted on a motherboard fixture; this provides the R_{Total}. The resistance requirement, R_{Req}, may be calculated for each chain as explained in Section 4.2, "Determination of Maximum Electrical Resistance" on page 21.

Figure 3. Methodology for Measuring Total Electrical Resistance

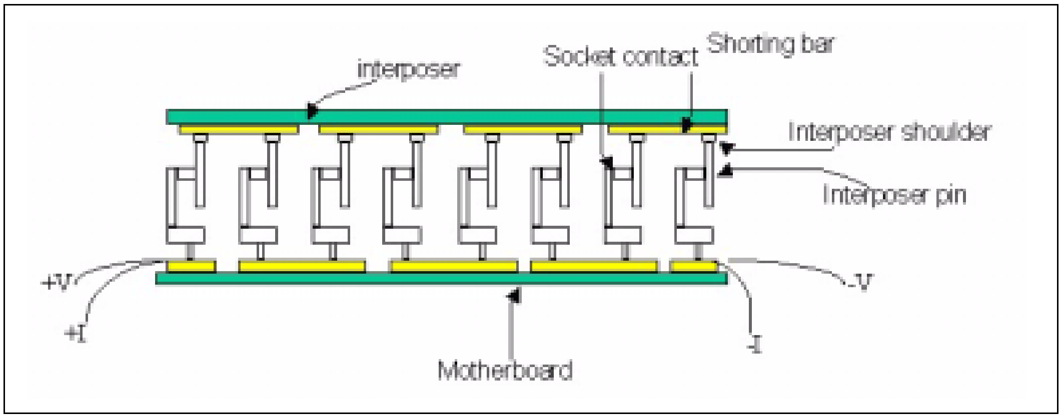


Figure 4. Methodology for Measuring Electrical Resistance of the Jumper

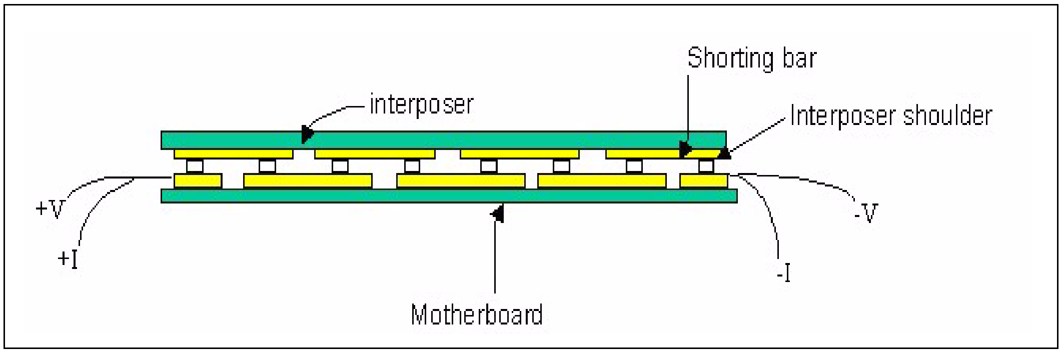


Figure 5 shows the resistance test fixtures separately and superimposed. The upper figure is the package. The next figure is the baseboard. There are 48 daisy chain configurations on resistance test board. The bottom figure is the two parts superimposed. Table 5 shows these configurations with the number of pins per each chain and netlist.

Figure 5. Electrical Resistance Fixtures Superimposed

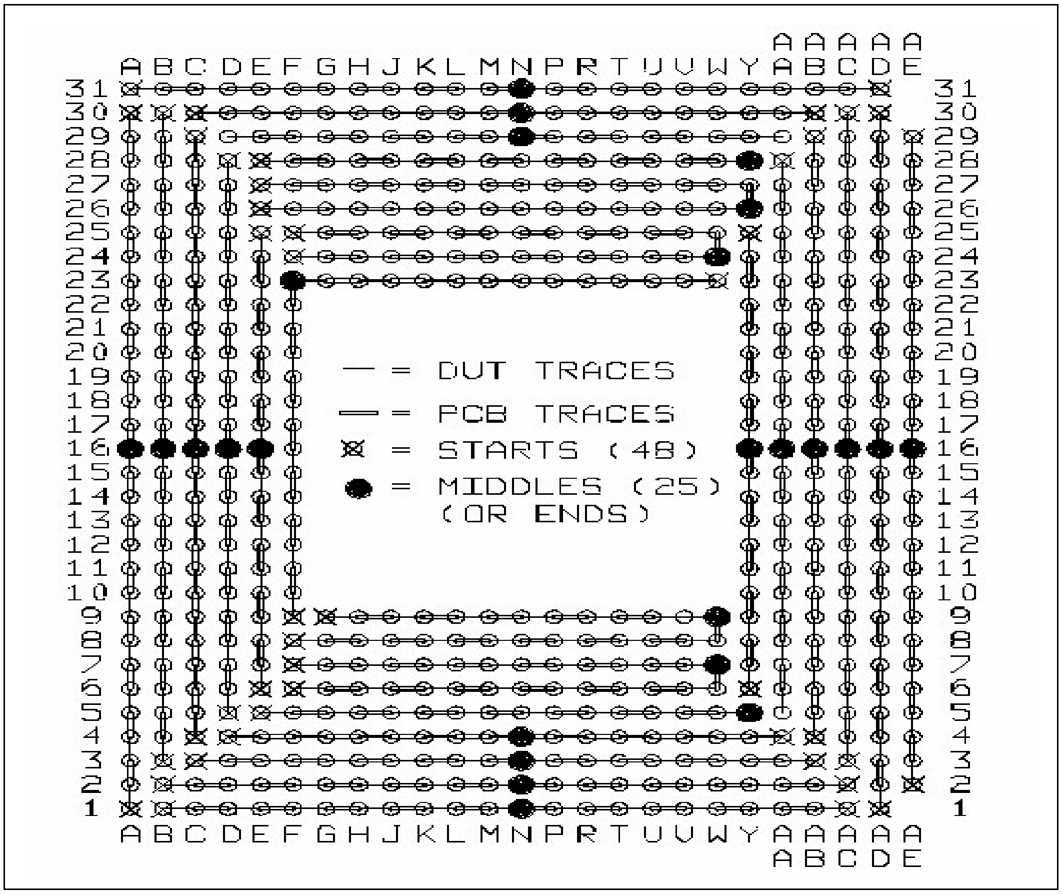


Table 5. Resistance Test Fixtures Netlist (Sheet 1 of 2)

		DC Endpoints		Edgefingers: Hi		Edgefingers: Low	
Daisy Chain	Number of Pins per Chain	Hi	Low	+I	+V	-V	-I
1	14	AE2	AE16	A94	A93	A118	A117
2	14	AE29	AE16	A136	A135	A118	A117
3	16	AD1	AD16	A92	A91	A116	A117
4	14	AD30	AD16	A138	A137	A116	A117
5	14	AC3	AC16	A96	A95	A114	A113
6	14	AC30	AC16	A142	A141	A114	A113
7	12	AB4	AB16	A98	A97	A112	A111
8	14	AB29	AB16	A134	A133	A112	A111
9	12	AA5	AA16	A100	A99	A110	A109
10	12	AA28	AA16	A132	A131	A110	A109
11	10	Y6	Y16	A102	A101	A108	A107

Table 5. Resistance Test Fixtures Netlist (Sheet 2 of 2)

		DC Endpoints		Edgefingers: Hi		Edgefingers: Low	
Daisy Chain	**Number of Pins per Chain**	**Hi**	**Low**	**+I**	**+V**	**-V**	**-I**
12	10	Y25	Y16	A130	A129	A108	A107
13	10	AC1	N1	A90	A89	A46	A45
14	12	B1	N1	A64	A63	A46	A45
15	10	AC2	N2	A88	A87	A48	A47
16	12	B2	N2	A66	A67	A48	A47
17	10	AB3	N3	A86	A85	A50	A49
18	10	C3	N3	A68	A67	A50	A49
19	8	AA4	N4	A84	A83	A52	A51
20	10	D4	N4	A70	A69	A52	A51
21	16	E5	Y5	A72	A71	A120	A119
22	14	F6	W7	A74	A73	A104	A103
23	14	F7	W7	A76	A75	A104	A103
24	14	F8	W9	A78	A77	A106	A105
25	12	G9	W9	A82	A81	A106	A105
26	16	A1	A16	A62	A61	A42	A41
27	46	A30	A16	A18	A17	A42	A41
28	14	B3	B16	A60	A59	A40	A39
29	14	B30	B16	A14	A13	A40	A39
30	12	C4	C16	A58	A57	A38	A37
31	14	C29	C16	A20	A19	A38	A37
32	12	D5	D16	A56	A55	A36	A35
33	12	D28	D16	A22	A21	A36	A35
34	10	E5	E16	A72	A71	A44	A43
35	10	E25	E16	A24	A23	A44	A43
36	14	F9	F23	A80	A79	A28	A27
37	14	W23	F23	A128	A127	A28	A27
38	14	F24	W24	A26	A25	A126	A125
39	14	F25	W24	A2	A1	A126	A125
40	16	E26	Y26	A4	A3	A124	A123
41	16	E27	Y26	A6	A5	A124	A123
42	16	E28	Y28	A8	A7	A122	A121
43	10	D29	N29	A10	A9	A34	A33
44	8	AA29	N29	A146	A145	A34	A33
45	10	C30	N30	A12	A11	A32	A31
46	10	AB30	N30	A144	A143	A32	A31
47	12	A31	N31	A16	A15	A30	A29
48	12	AD31	N31	A140	A139	A30	A29

4.2 Determination of Maximum Electrical Resistance

This section provides a guideline for the instruments used to take the measurements.

Note: The instrument selection should consider the guidelines in EIA 364-23A.

1. These measurements use a four-wire technique, where the instruments provide two separate circuits. One is a precision current source to deliver the test current. The other is a precision voltmeter circuit to measure the voltage drop between the desired points.
2. These separate circuits may be contained within one instrument, such as a high quality micro-ohmmeter, a stand-alone current source and voltmeter, or the circuits of a data acquisition system.
3. Measurement accuracy in ohms is specified as ± 0.1% of reading, or ± 0.1 mΩ, whichever is greater. The vendor is responsible for demonstrating that their instrument(s) may meet this accuracy.
4. Automation of the measurements may be implemented by scanning the chains through the edge or cable test connector using a switch matrix. The matrix may be operated by hand, or through software.
5. Measure R_{Total} for each daisy chain of ‘package + socket + motherboard’ unit.
6. Measure R_{jumper} for each daisy chain of 30 ‘package + motherboard’ units. Calculate for each daisy chain. (There is 30 data for each daisy chain.)
7. For each socket unit, use the formula in Equation 1 to calculate $R_{Req.}$

Equation 1. Calculation of R_{Req}

$$R_{Req} = \frac{R_{Total} - \bar{R}_{jumper}}{N}$$

R_{Req} is the average contact resistance for socket pin.

4.3 Inductance

The bottom fixture for the inductance measurement is a ground plane on the secondary side of the motherboard with all pins grounded. The component side of the socket PCB does not contain a plane. The top fixture is the package, which contains pins that may connect to the socket. Figure 6 shows the inductance measurement fixture cross-section and the inductance measurement methodology. The first figure shows the entire assembly. The second figure shows the assembly without the socket; the socket-seating plane of the package is directly mounted to the component side of the socket PCB. This is used to calibrate out the fixture contribution. The materials for the fixture must match the materials used in the processor. Note the probe pad features exist on the topside of the top fixture, and the shorting plane exists only on the bottom side of the bottom fixture. Figure 7 presents the inductance and capacitance fixture design.

Figure 6. Inductance Measurement Fixture Cross-Section

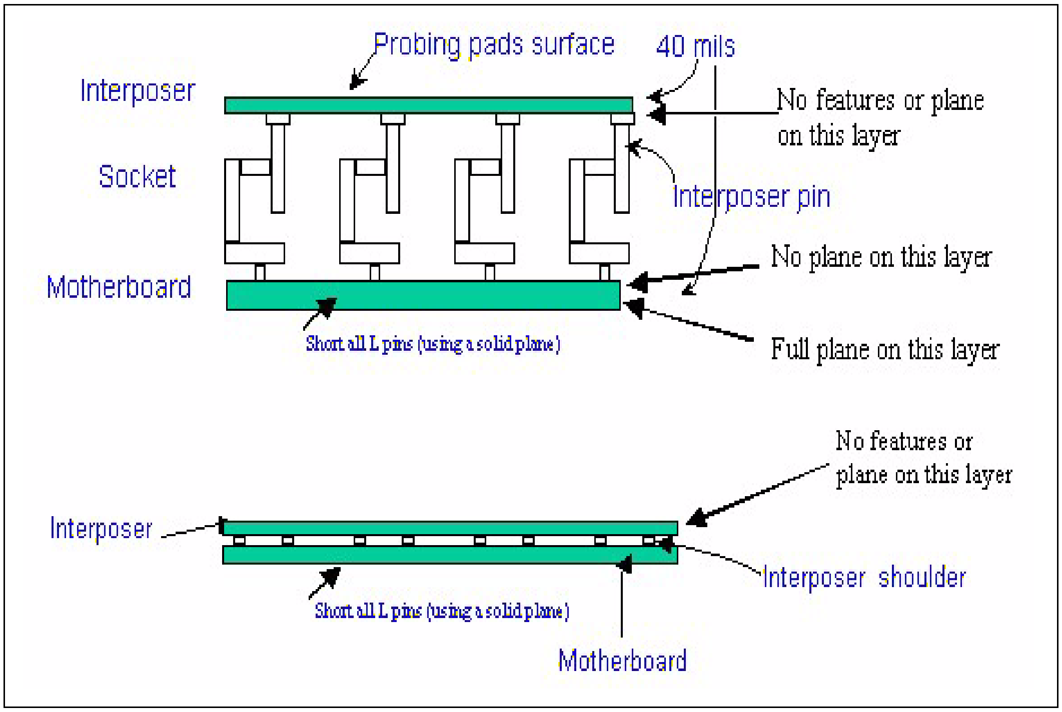
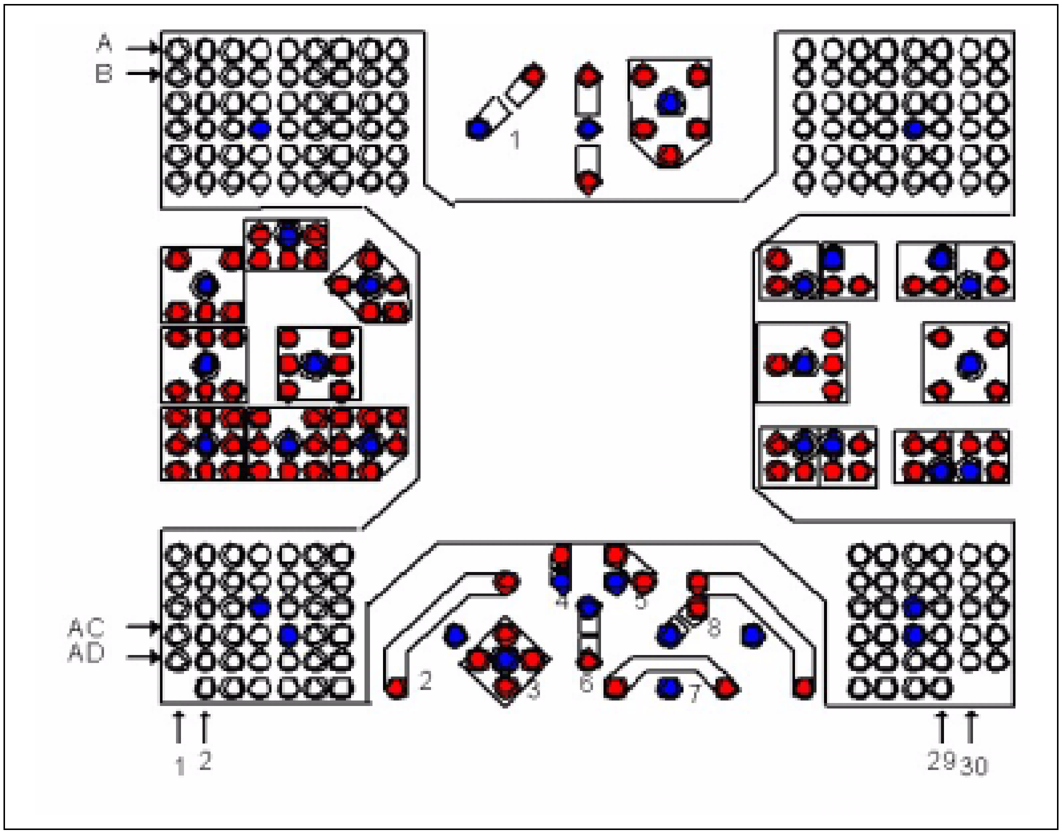


Figure 7. Inductance and Capacitance Fixture Cross-Section



4.3.1 Design Procedure for Inductance Measurements

The measurement equipment required to perform the validation is:

- Hewlett-Packard* HP8753D Vector Network Analyzer (VNA) or equivalent
- Robust* Probe Station (GTL4040) or equivalent
- Probes - GS1250 and GSG1250 Air-Co-Planar* or equivalent
- Calibration – Cascade* Calibration Substrates or equivalent
- Measurement objects - Packages, sockets, motherboards

4.3.1.1 Measurement Steps

1. Equipment Setup
   a. Cables must be connected to the network analyzer and to the probes using the appropriate torque wrench to ensure consistent data collection every time the measurement is performed.
2. Set VNA
   a. Bandwidth = 300 KHz – 3 GHz with 801 points
   b. Averaging Factor = 16

3. Perform Open/Short/Load calibration.
   a. Perform calibration at the start of any measurement session.
   b. Create Calibration Kit when necessary for the first time.
   c. Do not perform port extension after the calibration.
4. Check to ensure calibration is performed successfully.
5. Measure the inductance of Configuration 4 of the package mounted on the socket, which is mounted to the motherboard fixture (see Figure 7).
   a. Call this $L_{socket\ assembly}$.
   b. Export data into MDS/ADS. Capture data at frequency specified in Section 6 of Table 3.
6. Measure the inductance of Configuration 4 of the package mounted on the socket, which is mounted to the motherboard fixture (see Figure 7). Call this $L_{sandwich}$.
   a. Measure 30 units.
   b. The package for 30 units must be chosen from different lots. Use five different lots, with six units from each lot.
   c. Export data into MDS/ADS. Capture the data at frequency specified in Section 6 of Table 3.
   d. Calculate $\overline{L}_{sandwich}$.
   e. For each socket unit, use Equation 2 to calculate L_{socket}.

Equation 2. Calculation of L_{socket}

$$L_{socket} = L_{socket\ assembly} - \overline{L}_{sandwich}$$

The equation indicates that $\overline{L}_{sandwich}$ is subtracted from each $L_{socket\ assembly}$ and the result may be compared with specification value for each individual socket unit.

4.3.2 Correlation of Measurement and Model Data Inductance

To correlate the measurement and model data for loop inductance, one unit of measured socket assembly (socket and shorted test fixture) and one unit of measured sandwich (shorted test fixture) may be chosen for cross sectioning. Both units may be modeled based on data from cross sectioning using Ansoft* 3D. The sandwich inductance may be subtracted from socket assembly inductance for both measured and modeled data. This procedure results in loop inductance for socket pin + interposer pin. This final result may be compared with the loop inductance from the supplier model for the socket. The shoulder of the interposer is not included in the electrical modeling. When there is any difference between them, it will be called the de-embedded correction factor. Adding the interposer to the socket and then eliminating the contribution of the fixture creates this correction factor because inductance is not linear.

4.4 Pin-to-Pin Capacitance

Pin-to-pin capacitance shall be measured using Configuration 4, with the motherboard not connected, and only the measurements with the package mounted on the socket may be taken. Capture data at frequency specified in Section 5 of Table 3.

4.5 Dielectric Withstand Voltage

No disruptive discharge or leakage greater than 0.5 mA is allowed when subjected to 360 V_{RMS}. The sockets shall be tested according to EIA-364, Test Procedure 20A, Method 1. The sockets shall be tested unmounted and unmated. Barometric pressure shall be equivalent to sea level. The sample size is 25 contact-to-contact pairs on each of four sockets. The contacts shall be randomly chosen.

4.6 Insulation Resistance

The Insulation Resistance shall be greater than 800 MΩ when subjected to 500 VDC. The sockets shall be tested according to EIA-364, Test Procedure 21. The sockets shall be tested unmated and unmounted. The sample size is 25 contact-to-contact pairs on each of four sockets. The contacts shall be randomly chosen.

4.7 Contact Current Rating

Measure and record the temperature rise when the socket is subjected to rated current of 0.8 A. The sockets shall be tested according to EIA-364, Test Procedure 70A, Test Method 1. The sockets shall be mounted on a test-board and mated with a package so those 603 pins are connected in series. The recommended test board is the FSETV4 Revision 1 and the recommended package is FSETV5 Revision 1. Table 6 presents the wiring list. Mount the thermocouple as near to contact N3 or N7 as possible. Short the daisy chains by means of the edge fingers when possible. The sample size is one socket.

Table 6. Netlist for FSETV4 Revision 1 Edge Fingers

Edge Fingers	Jumpers		
+I: A61			
-I: A145	A85-A89	A45-A17	A135-A141
	A59-A57	A129-A133	A7-A5
	A87-A95	A15-A13	A139-A143
	A49-A47	A131-A137	A3-A1
	A101-A99	A11-A9	

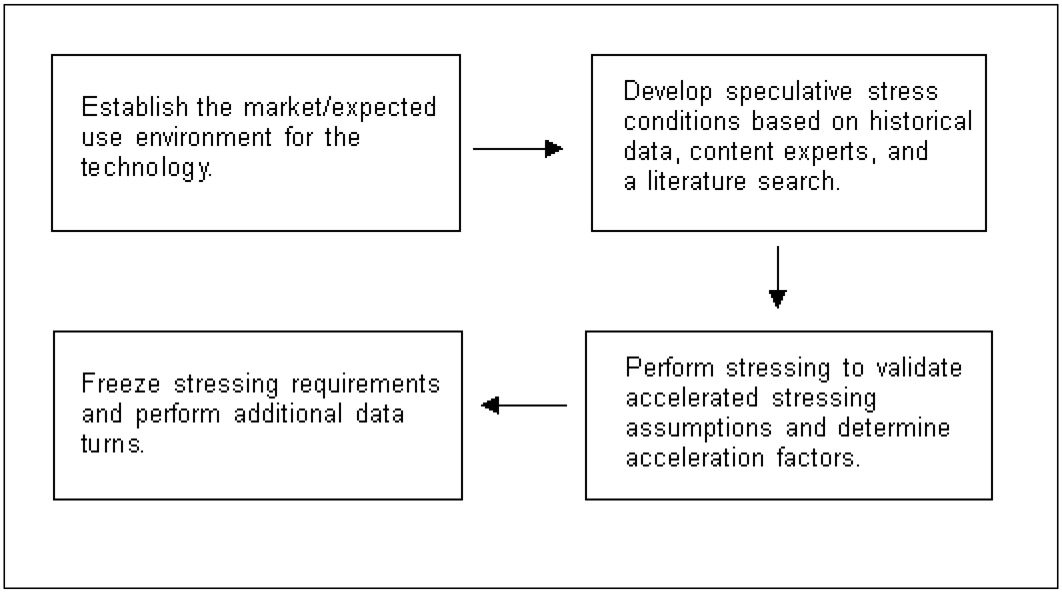
This page intentionally left blank.

5.0 Environmental Requirements

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points.

The reliability targets in this section are based on the expected field use environment for a desktop product. The test sequence for new sockets will be developed using the knowledge-based reliability evaluation methodology, which is acceleration factor dependent. A simplified process flow of this methodology may be seen in Figure 8.

Figure 8. Flowchart of Knowledge-Based Reliability Evaluation Methodology



A detailed description of this methodology may be found at:
http://developer.intel.com/design/packtech/245162.htm

The use environment expectations assumed are for desktop processors, based on an expected life of seven to ten years, are listed in Table 7. The target failure rates are <1% at seven years and <3% at ten years.

Table 7. Use Conditions Environment (Sheet 1 of 2)

Use Environment	Speculative Stress Condition	Seven Year Life Expectation	Ten Year Life Expectation
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated).	Temperature Cycle	1500 cycles with a mean ΔT = 40 °C	2150 cycles with a mean ΔT = 40 °C
High ambient moisture during low-power state (operating voltage).	THB / HAST	62,000 hrs at 30 °C, 85% RH	89,000 hrs at 30 °C, 85% RH
High operating temperature and short duration high temperature exposures.	BAKE	62,000 hrs at Tjmax	89,000 hrs at Tjmax
Fast, large gradient on/off to max operating temp. (power cycle or internally heated including power save features).	Power Cycle	7,500 cycles	11,000 cycles

Table 7. Use Conditions Environment (Sheet 2 of 2)

Use Environment	Speculative Stress Condition	Seven Year Life Expectation	Ten Year Life Expectation
Shipping & Handling	Mechanical Shock 50g trapezoidal profile; 170 inches/sec Velocity change; 11 msec duration pulse	3 drops/axis, 6 axes	
Shipping & Handling	Random Vibration 3.13 gRMS, random, 5 Hz - 20 Hz .01 g2/Hz sloping up to .02 g2/Hz 20 Hz - 500 Hz .02 g2/Hz	10 min/axis, 3 axes	

5.1 Porosity Test

5.1.1 Porosity Test Method

Use EIA 364, Test Procedure 53A, nitric acid test. Perform the porosity test on 20 contacts, randomly selected per socket, five sockets.

5.1.2 Porosity Test Criteria

The porosity test criteria includes a maximum of two pores per set of 20 contacts, as measured per EIA 364, Test Procedure 60.

5.2 Plating Thickness

Measure various plating thickness on contact surface per EIA 364, Test Procedure 48, Method C or Method A. Perform the plating thickness test on 20 randomly selected contacts per socket, five sockets. No plating thickness measured shall be less than the minimum plating thickness specified in Section 3.9.3, “Contact Area Plating” on page 13.

5.3 Solvent Resistance

Requirement: No damage to ink markings when applicable. EIA 364-11A.

5.4 Solderability

(Applicable for leaded sockets) Requirement: 95% coverage per ball/surface mount feature. EIA 364, Test Procedure 52, Class 2, Category 3. Perform the solderabilty test on 20 randomly selected contacts per socket, five sockets.

5.5 Durability

Use per EIA 364, test procedure 09B. The same package pin field is to be used for cycles one through 51. Measure contact resistance when mated in cycles one and 51. A spare package pin field is used for cycles two through 50. A pair of new package pin fields to be used for each of the socket samples. The package should be removed at the end of each de-actuation cycle and reinserted into the socket.

This page intentionally left blank.

6.0 Validation Testing Requirements

This section of the document outlines the tests that must be successfully completed in order for the supplier's socket to pass the design guidelines validation. It provides the test plan and procedure required for validation.

6.1 Applicable Documents

- EIA-364-C
- *Low Voltage Intel® Xeon™ Processor at 1.60 GHz Datasheet* (order number 273766-001)
- *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 to 2.40 GHz Datasheet* (order number 298642-003)
- Thermal Design Guidelines Documents

Note: For details on ordering this documentation, visit the Intel World Wide Web site at http://www.intel.com or contact your Intel field sales representative

6.2 Testing Facility

Testing will be performed by an Intel designated test facility.

6.3 Funding

Socket supplier will fund socket validation testing for their socket. Any additional testing that is required due to design modifications will also be at the expense of the supplier.

6.4 Socket Design Verification

At the earliest possible date, a detailed drawing of the socket supplier's 604-pin Socket must be provided to Intel for review. This drawing should include all of the features called out in this design guideline (marking, pinout, cam location, date code location and explanation, etc.) as well as dimensional and board layout information. This drawing will be used to confirm compliance to this design guideline.

6.5 Reporting

Test reports of the socket validation testing will be provided directly from the independent test facility to Intel. Intel will also be given access to contact the test facility directly to obtain socket validation status, explanation of test results and recommendations based on the test results.

6.6 Process Changes

Any significant change to the 604-pin Socket will require submission of a detailed explanation of the change at least 60 days prior to the planned implementation. Intel will review the modification and establish the necessary re-validation procedure that the socket must pass.

Note: Any testing that is required MUST be completed before the change is implemented.

Typical examples of significant changes include, **but are not limited to, the following:** Plastic material changes including base material or color; contact changes including base material, plating material or thickness; and design modifications.

6.7 Quality Assurance Requirements

The OEM’s will work with the socket supplier(s) they choose to ensure socket quality.

6.8 Socket Test Plan

6.8.1 Submission of a 604-pin Socket for Validation Testing

The socket supplier's 604-pin Socket will be sent to an Intel designated independent test facility for socket validation testing. The sockets submitted must be according to the sample lots required in Section 6.4, “Socket Design Verification” on page 31. Refer to Section 6.11, “Production Lot Definition” on page 32 and Section 6.12, “Socket Validation” on page 33 for production lot definitions and the number of samples required for validation testing.

6.9 Mechanical Samples

A mechanical sample of 604-pin Socket, package, and heat sink (or suitable mockups that approximate size and mass of the planned heat sink) will be used during the mated socket validation testing. The maximum mass for 604-pin Socket package heat sink is recommended as (but not limited to) 450 grams with the stipulation that the requirements of Section 3.1, “Mechanical Supports” on page 11 be met. See data sheet and related documentation for further information on heat sinks, thermal solutions and mechanical support.

6.10 Socket Validation Notification

Upon completion of the testing and receipt of test data, Intel and/or the Intel designated test facility will prepare a summary report for the socket supplier and Intel that will provide notification as to whether the socket has passed or failed socket validation testing.

6.11 Production Lot Definition

A production lot is defined as a separate process run through the major operations including molding, contact stamping, contact plating and assembly. These lots should be produced on separate shifts or days of the week. Lot identification marking must be provided to Intel as verification of this process.

6.12 Socket Validation

Socket validation must meet or exceed all guidelines called out in this specification that include:

- Visual Inspection
- CTF Dimensional Verification
- Electrical Resistance
- Loop Inductance
- Pin to Pin Capacitance
- Contact Current Rating
- Dielectric Withstand Voltage
- Insulation, Durability
- Porosity
- Plating Thickness
- Solvent Resistance (when applicable)
- Solderability (applicable for leaded sockets)
- Post Reliability Visual
- Use Conditions

The use conditions target failure rates are <1% at seven years and <3% at ten years. Statistical sample sizes, taken randomly from multiple lots, for each test is required.

This page intentionally left blank.

7.0 Safety Requirements

Design, including materials, shall be consistent with the manufacture of units that meet the following safety standards:

- UL 1950, most current editions
- CSA 950, most current edition
- EN60 950, most current edition and amendments
- IEC60 950, most current edition and amendments

This page intentionally left blank.

8.0 Documentation Requirements

The socket supplier shall provide Intel with the following documentation:

- Multi-line coupled SPICE models for socket.
- Product design guideline incorporating the requirements of these design guidelines.
- Recommended board layout guidelines for the socket consistent with low cost, high volume printed circuit board technology.

The test facility shall provide Intel and the supplier with the Validation Testing and Test Report supporting successful compliance with these design guidelines.

This page intentionally left blank.

Appendix A

Schematics are provided for the 604-pin package assembly, mPGA604 Socket, and 603-pin interposer assembly. Listed below are the schematics included for each assembly and socket.

Figure 9. 42.5 mm, 604-Pin Package Assembly Drawing

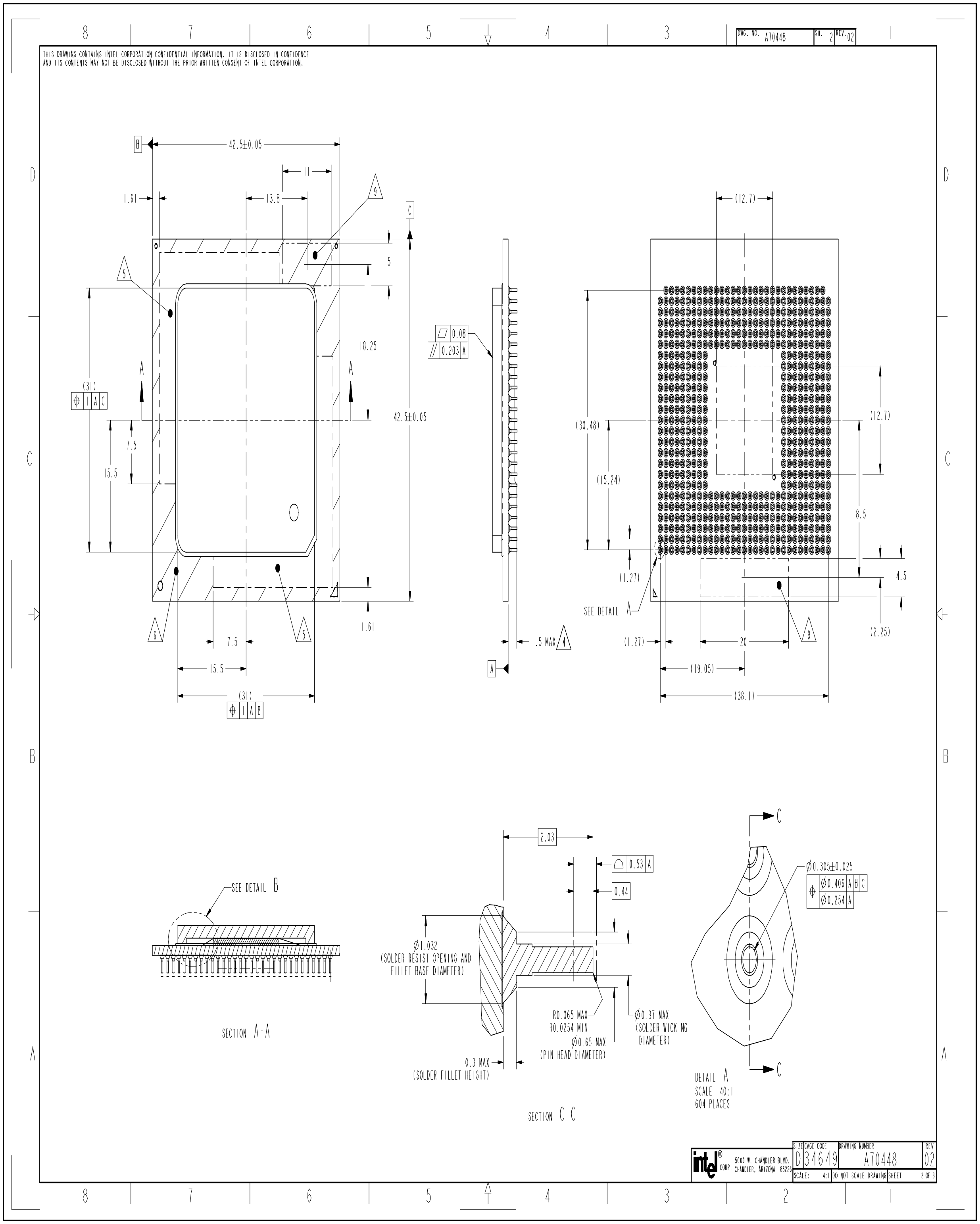
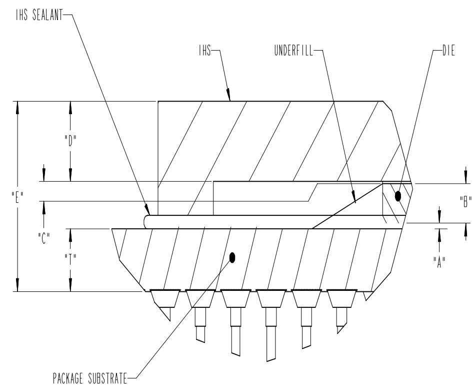


Figure 10. 42.5 mm, 604-Pin Package Assembly Drawing with Package Detail

DWG. NO. A70448 SH. 3 REV. 02



DETAIL B
SCALE 20:1

ITEM	DIMENSION
T	1.17±0.07 (8 LAYER FCPGA2) 8
A	0.1±0.025
B*	0.74±0.025
C	0.038±0.012
D	1.5±0.05
E*	3.548±0.182(WC), 3.548±0.094(RSS)

* ADD 0.05mm FOR 300mm WAFERS

intel CORP. 5000 W. CHANDLER BLVD. CHANDLER, ARIZONA 85226

SIZE	CAGE CODE	DRAWING NUMBER	REV
D	34649	A70448	02
SCALE: NONE	DO NOT SCALE DRAWING	SHEET 3 OF 3	

Figure 11. mPGA604 Socket Drawing

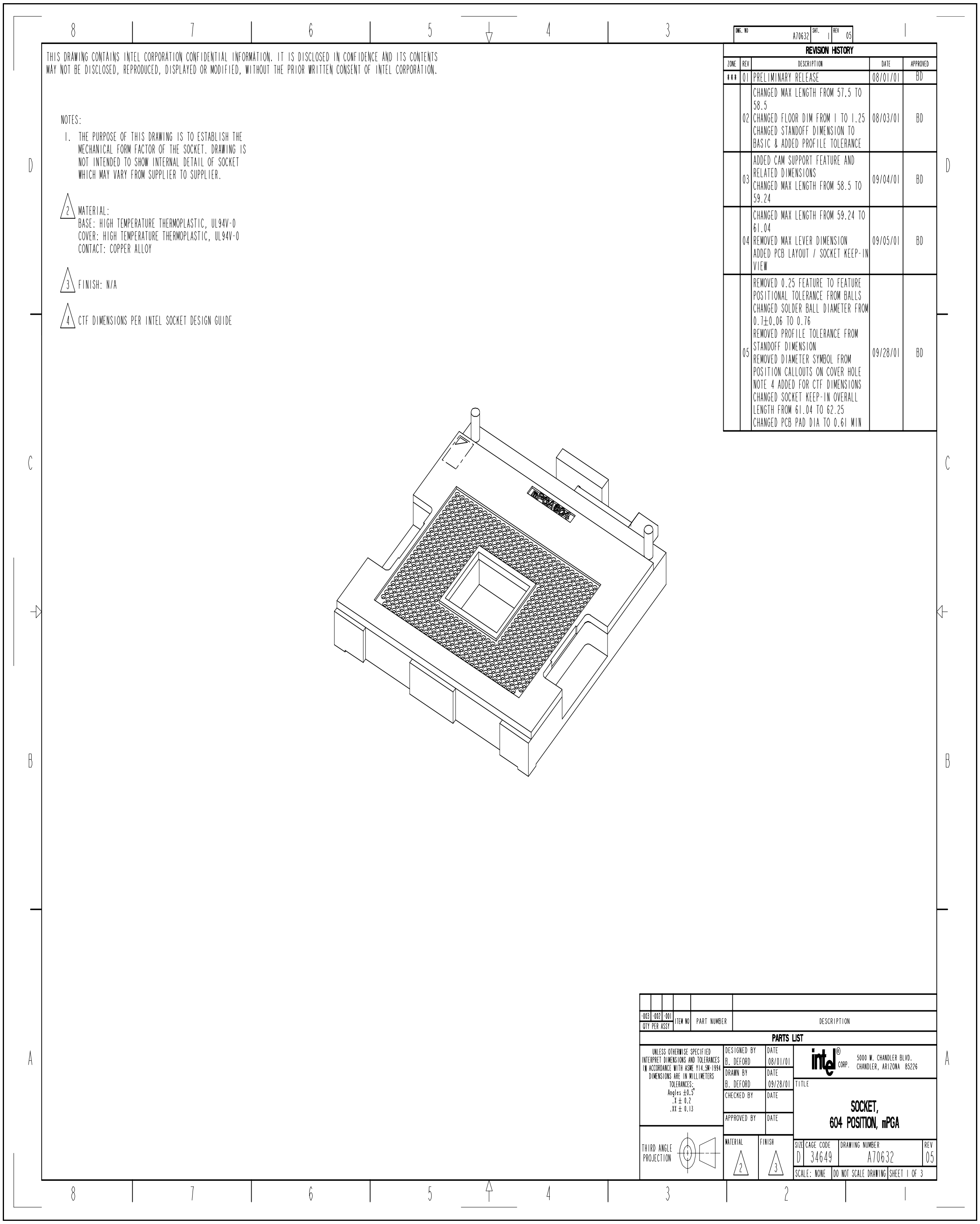


Figure 12. mPGA604 Socket Drawing with Dimensions

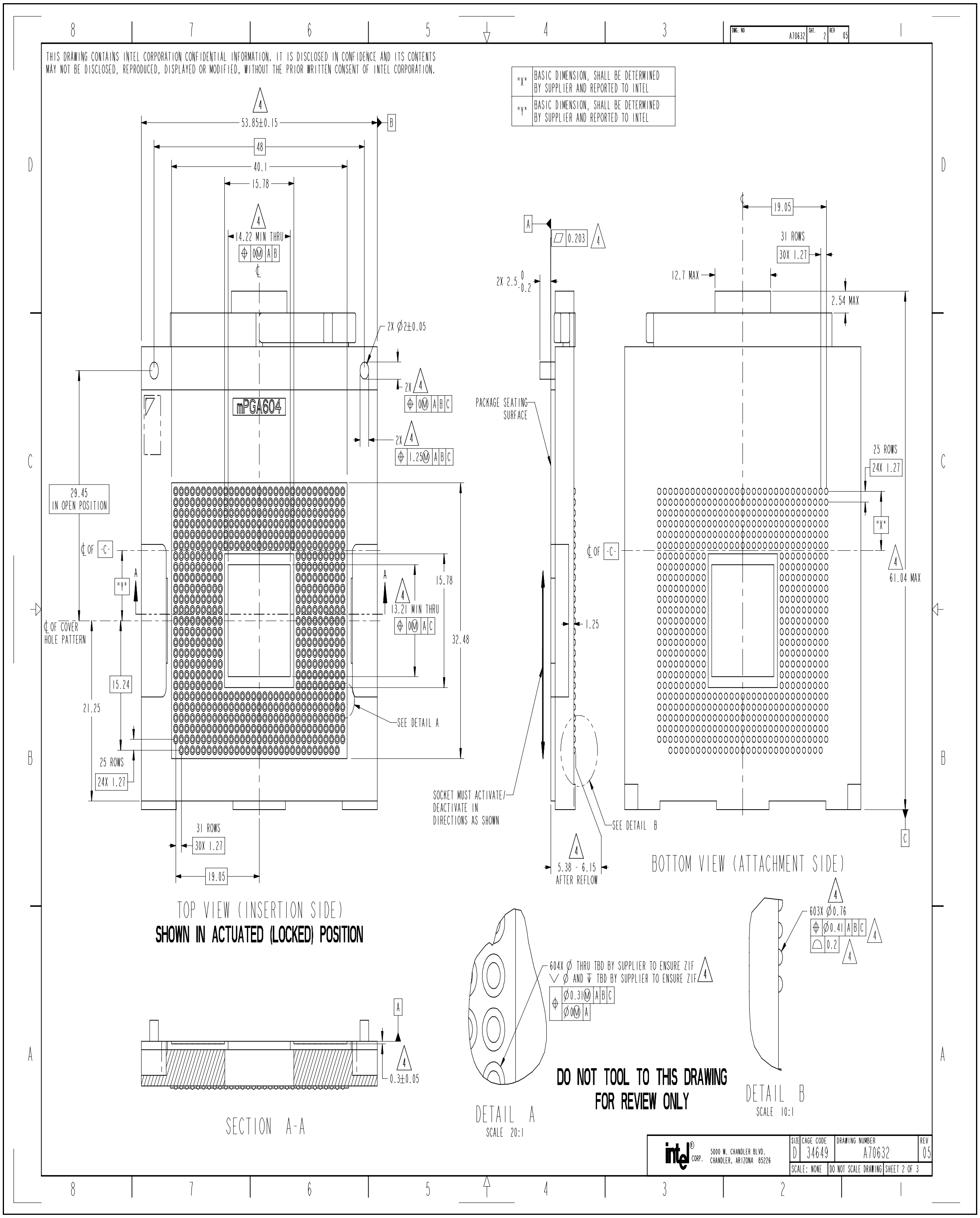


Figure 13. mPGA604 Socket Drawing with Dimensions (Continued)

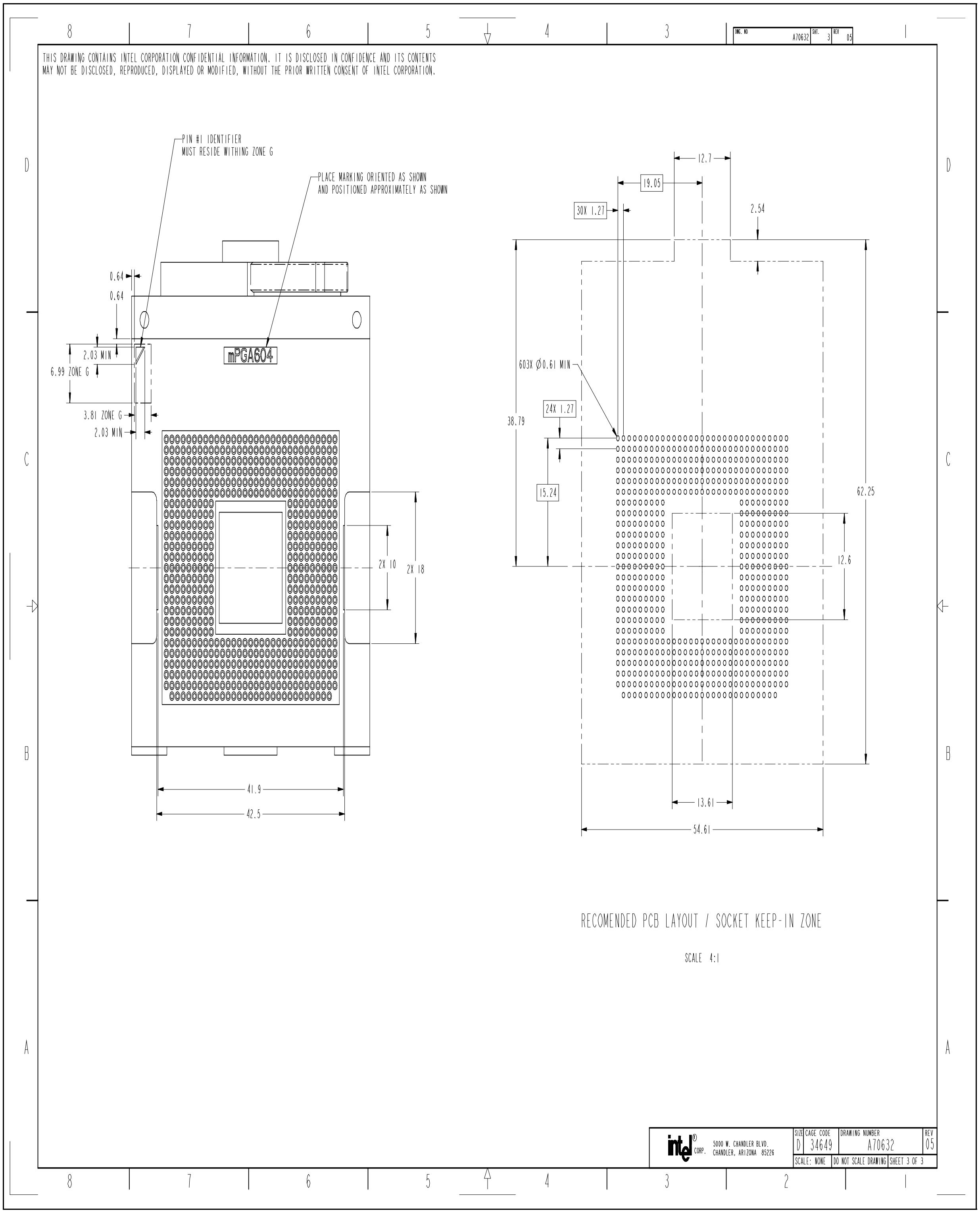


Figure 14. 603-Pin Interposer Assembly Drawing with Dimensions

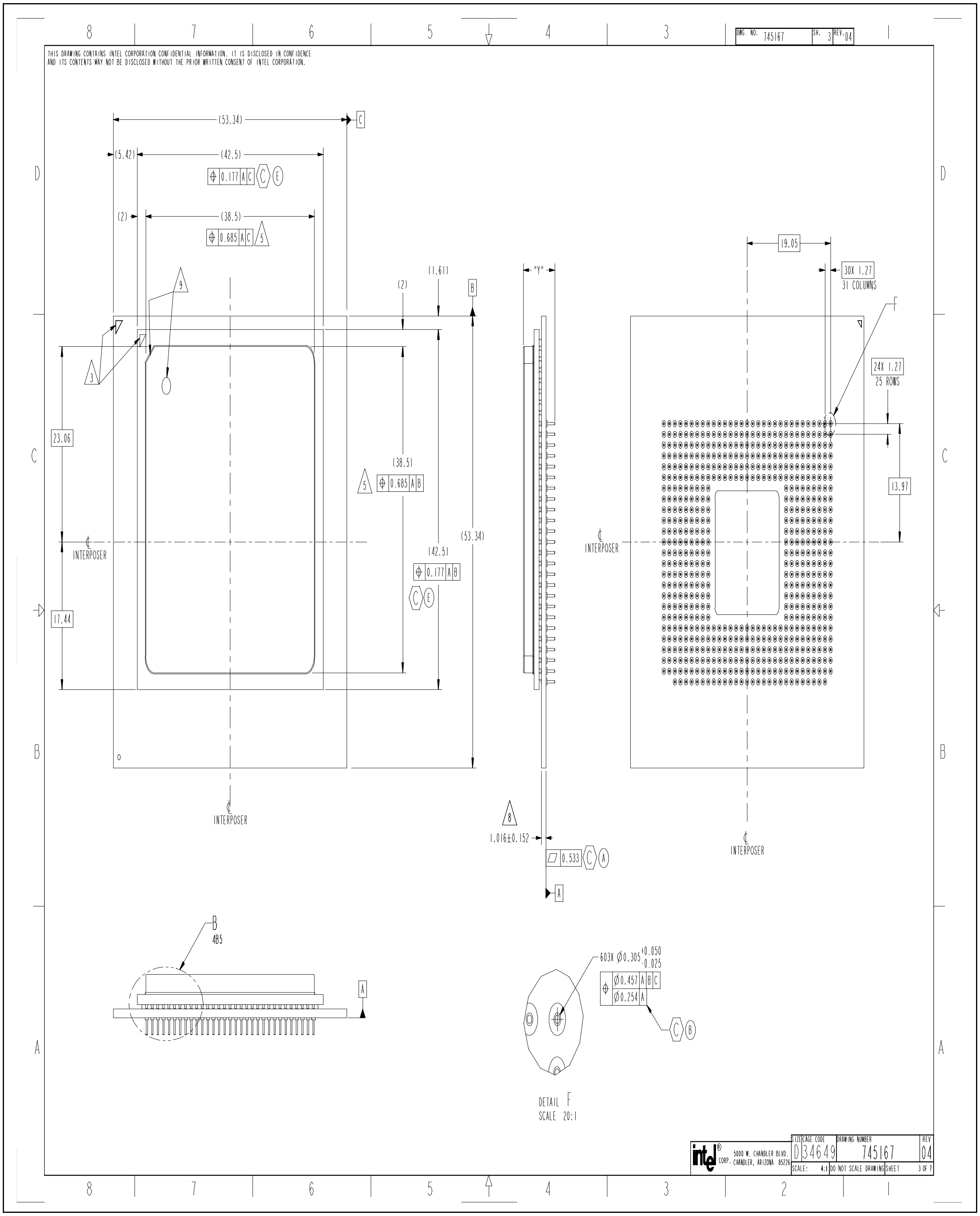
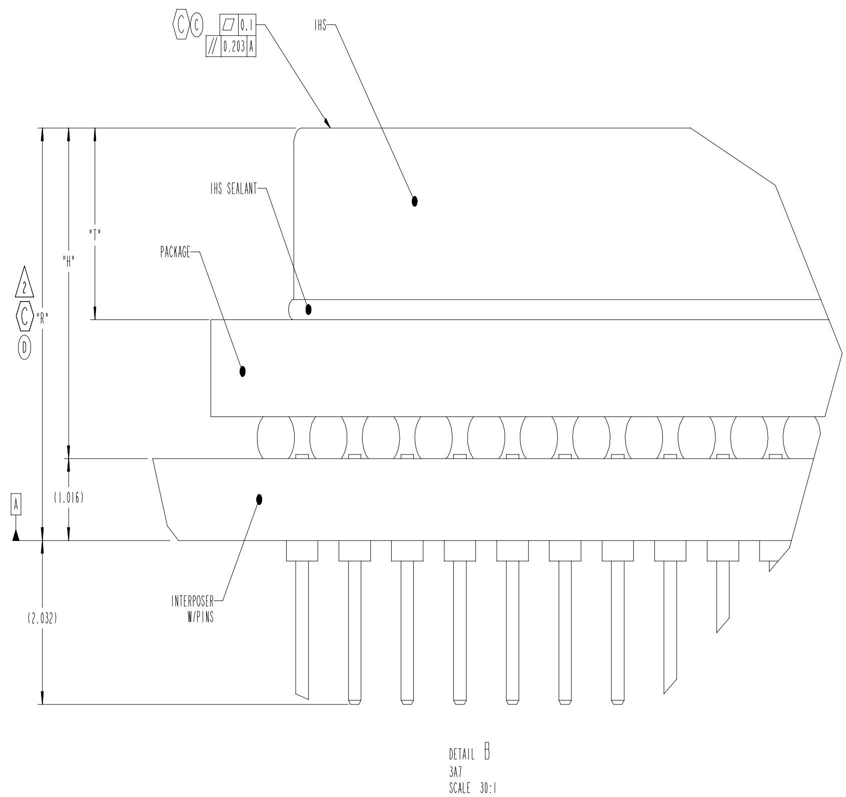


Figure 15. 603-Pin Interposer Assembly Drawing with Dimension (Continued)



ITEM	8 LAYER OLGA WITH 1.5mm IHS AND POLYMER TIM	8 LAYER FCBGA2 WITH 1.5mm IHS AND POLYMER TIM	8 LAYER FCBGA2 WITH 3mm IHS AND POLYMER TIM	10 LAYER FCBGA2 WITH 1.5mm IHS AND POLYMER TIM	10 LAYER FCBGA2 WITH 3mm IHS AND POLYMER TIM	8 LAYER FCBGA2 WITH 3mm IHS AND SOLDER TIM	10 LAYER FCBGA2 WITH 3mm IHS AND SOLDER TIM
"T"*	(2.378) ±0.112 (WC) ±0.062 (RSS)	(2.378) ±0.112 (WC) ±0.062 (RSS)	(3.878) ±0.112 (WC) ±0.062 (RSS)	(2.378) ±0.112 (WC) ±0.062 (RSS)	(3.878) ±0.112 (WC) ±0.062 (RSS)	(3.992) ±0.176 (WC) ±0.13 (RSS)	(3.992) ±0.176 (WC) ±0.13 (RSS)
"H"*	(4.014) ±0.348 (WC) ±0.178 (RSS)	(3.984) ±0.298 (WC) ±0.149 (RSS)	(5.484) ±0.298 (WC) ±0.149 (RSS)	(4.074) ±0.338 (WC) ±0.172 (RSS)	(5.574) ±0.338 (WC) ±0.172 (RSS)	(5.598) ±0.362 (WC) ±0.223 (RSS)	(5.688) ±0.402 (WC) ±0.25 (RSS)
"R"*	(5.03) ±0.5 (WC) ±0.234 (RSS)	(5) ±0.45 (WC) ±0.213 (RSS)	(6.5) ±0.45 (WC) ±0.213 (RSS)	(5.09) ±0.49 (WC) ±0.229 (RSS)	(6.59) ±0.49 (WC) ±0.229 (RSS)	(6.614) ±0.514 (WC) ±0.301 (RSS)	(6.704) ±0.554 (WC) ±0.322 (RSS)
"Y"*	(7.062)	(7.032)	(8.532)	(7.122)	(8.622)	(8.646)	(8.736)

* ADD 0.05 FOR 300mm WAFER PRODUCTS

intel® CORP. 5000 W. CHANDLER BLVD. CHANDLER, ARIZONA 85226

SIZE	CAGE CODE	DRAWING NUMBER	REV
D	34649	745167	04
SCALE: NONE	DO NOT SCALE DRAWING	SHEET	4 OF 7